Basics

- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results

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GaN Enhancement mode High Electron Mobility Transistor (E-HEMT):

- Lateral 2DEG (2-dimensional electron gas) channel formed between AlGaN and GaN layers
- Positive gate bias opens up 2DEG channel
- 0V or negative gate voltage shuts off 2DEG and block forward conduction
- Voltage driven: Gate driver charges/discharges (C_{GD} + C_{GS})
- No DC gate driving current needed: gate leakage current only (I_{GSS})
Gate Characteristics GaN E-HEMT vs. other technologies

- Similar gate drive requirement to Silicon MOSFET/IGBT
- Much Smaller gate charge – Lower drive loss, faster rise & fall time
- **Lower gate voltage – Select right gate driver UVLO**
- Easy 5 to 6.5V gate drive with maximum rating +7V and +10V transient
- 0V to turn off, typical $V_{GTH}=1.5V$
- Negative voltage improves gate drive robustness but optional
- Easy slew rate control using gate resistor

<table>
<thead>
<tr>
<th>Gate drive voltage level</th>
<th>GaN Systems GaN E-HEMT</th>
<th>Si MOSFET</th>
<th>IGBT</th>
<th>SIC MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum rating</td>
<td>-10/+7V</td>
<td>+/-20V</td>
<td>+/-20V</td>
<td>-8/+18V</td>
</tr>
<tr>
<td>Transient maximum</td>
<td>-20/+10V*</td>
<td></td>
<td>+/-30V</td>
<td></td>
</tr>
<tr>
<td>Typical operational values</td>
<td>0 or -3/+5-6.5V</td>
<td>0/+10-12V</td>
<td>0 or -9/+15V</td>
<td>-4/+15V</td>
</tr>
</tbody>
</table>

[*] pulse width < 1µS
GaN E-HEMT Reverse Conduction

- No parasitic body diode: **Zero $Q_{RR}$** Loss & very **high dv/dt** ruggedness
- GaN E-HEMT is naturally capable of reverse conduction, **without external diode**
- Unlike MOSFETs/IGBT, reverse current flow through same 2DEG channel as forward conduction
- “Diode” like reverse behavior is $V_{GS}$ dependent

**Drain-source forward bias:**

**Reverse bias $V_{GS}$=0V:**

- One can consider D/S swapped in reverse bias mode
- 2DEG channel starts to conduct when $V_{SD} = V_{GS'} (V_{GD}) > V_{GTH} = \sim 1.5V$
- Reverse current flows in 2DEG

**Reverse bias with $-V_{GS}$:**

- 2DEG starts to conduct when $V_{SD} = V_{GTH} + V_{GS\_OFF}$
- $-V_{GS}$ increases reverse voltage drop $V_{SD}$

When $V_{GS} \leq 0V$: no channel conduction
Reverse Conduction Loss model

**V_{GS} = 6V (on-state):**
- 2-quadrant bidirectional current flow in 2DEG channel
- Reverse R_{ds(on)} same as forward conduction
- \[ P_{loss\_rev} = I_{SD}^2 \times R_{DS(ON)}, Tj \]

**V_{GS} \leq 0V (off-state):**
- Modeled as “diode” with \( V_F \) + channel resistance \( R_{rev\_on} \) that is higher than \( R_{DS(ON)} \) in forward conduction
- \( V_{SD} \) increases with the negative gate voltage applied
- \[ P_{loss\_rev} = I_{SD}^2 \times R_{REV(ON)} + I_{SD} \times (V_{GTH} + V_{GS\_OFF}) \]

How does it affect the design:
- No external anti-parallel diode required
- No \( Q_{RR} \) Loss (\( Q_{OSS} \) loss only), perfect fit for half bridge where hard commutation is required – Higher efficiency and more robust without body diode
- Higher reverse conduction loss, for optimal efficiency:
  - Minimize dead time and utilize synchronous drive
  - Prefer 0V for turn-off
Reduce Losses using Dead time & Synchronous driving

- Synchronous driving with minimum dead time is recommended for optimum efficiency
- Dead time can be selected by considering the worst case gate driver propagation delay skewing + switching rise/fall time
  - For 650V GS66508T/P: typical 50-100ns
  - For 100V GS61008P: typical 15-20ns

25ns Delay difference for Si8261 Isolated gate driver

| Propagation Delay Difference | PDD | t_{PHMAX} - t_{PHMIN} | -1 | - | 25 ns |

Total switching time 26ns for GS66508T (R_G=10Ω, T_J=125°C)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-on delay time</td>
<td>t_{d(on)}</td>
<td>4.5</td>
<td>ns</td>
<td>V_{DD}=400V, V_{GS}=6V,</td>
</tr>
<tr>
<td>Rise time</td>
<td>t_r</td>
<td>6.3</td>
<td>ns</td>
<td>I_D=16A, R_G=10Ω</td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>t_{d(off)}</td>
<td>9.3</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>t_f</td>
<td>5.4</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
Design Considerations

- Basics
  - Design considerations
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Optimizing Gate Resistors

Select right gate resistance

- E-HEMT switching speed can be controlled by gate resistors
- $R_G$ is critical for optimum switching performance and gate drive stability
- Separate $R_G$ for turn-on and off is recommended

**Turn-on gate resistor $R_{GON}$:**

- Control the turn-on slew rate $\frac{dv}{dt}$
- For GS66508x: Recommended to start with $R_{GON} = 10\text{-}20\Omega$
- Too small $R_{GON}$: High $\frac{dv}{dt}$; drain current and $V_{GS}$ ringing
  - Higher switching loss due to gate ringing
  - Risk of miller turn-on and gate oscillation

**Turn-off gate resistor $R_{GOFF}$:**

- $R_{GOFF}$ smaller than $R_{GON}$ is recommended:
  - Provide strong pull-down for robust gate drive
- Typical value $R_{GOFF} = 1\text{-}3\Omega$
**Effect of R\textsubscript{GOFF} on power loss**

- Smaller R\textsubscript{GOFF} reduce E\textsubscript{OFF}.
- Too small R\textsubscript{GOFF} may create V\textsubscript{GS} undershoot and ringing:
  - Higher switching and dead time conduction loss
  - Potential gate oscillation
- Recommended to start with 1-3\(\Omega\) and adjust empirically

**Wide range of near zero E\textsubscript{OFF} can be easily achieved with GaN:**

- Extreme low Q\textsubscript{G} → 2DEG channel turns off fast enough → gate no longer controls turn-off V\textsubscript{DS} dv/dt (no plateau period)
- Turn-off dv/dt solely determined by how fast load current (L\textsubscript{OUT}) charges C\textsubscript{OSS}.
- Measured E\textsubscript{OFF} includes E\textsubscript{OSS}, which is NOT part of E\textsubscript{OFF} and will be dissipated at next turn-on transient.

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**GS66508P Measured E\textsubscript{ON}/E\textsubscript{OFF} (V\textsubscript{DS}=400V, R\textsubscript{GON}=10\(\Omega\), R\textsubscript{GOFF}=1\(\Omega\))**

- T\textsubscript{J}=25°C
- Near zero turn-off loss Id <15A
- GS66508P: E\textsubscript{oss}@400V = 7\(\mu\)J
- Minimum turn-off loss when Id <15A (R\textsubscript{GOFF} = 1\(\Omega\))
**Effect of $V_{GS}$ undershoot on dead time loss:**

- Example 48-12V Sync Buck $I_{SW} = 20A$ (GS61008P)
- LS $V_{GS}$ turn-off undershoot adds to the $V_{SD}$ drop during dead time $\rightarrow$ higher dead time loss
- Optimize $R_{GOFF}$ to balance between $E_{OFF}$ and dead time loss $\rightarrow$ more critical for VHF application and 100V device

$V_{SD} = 3.4V @ 20A$

Peak $V_{SD}$ bump caused by $V_{GS}$
GS66508P Switching Loss measurements

Switching energy loss tested on half bridge with inductive load:
*V_{DS} = 400V, V_{GS} = 6V, R_{G(ON)} = 10Ω, L_{P} = 10nH, L = 40uH, Gate driver IXDN609SI.*

<table>
<thead>
<tr>
<th>I_D (A)</th>
<th>$E_{ON}$ 25°C</th>
<th>$E_{OFF}$ 25°C</th>
<th>$E_{OFF}$ 25°C</th>
<th>$E_{ON}$ 125°C</th>
<th>$E_{OFF}$ 125°C</th>
<th>$E_{OFF}$ 125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_{G(OFF)}=10Ω$</td>
<td>$R_{G(OFF)}=1Ω$</td>
<td>$R_{G(OFF)}=1Ω$</td>
<td>$R_{G(OFF)}=10Ω$</td>
<td>$R_{G(OFF)}=1Ω$</td>
<td>$R_{G(OFF)}=1Ω$</td>
</tr>
<tr>
<td>5</td>
<td>27.8</td>
<td>7.1</td>
<td>7.0</td>
<td>30.0</td>
<td>7.2</td>
<td>7.1</td>
</tr>
<tr>
<td>10</td>
<td>36.7</td>
<td>12.7</td>
<td>7.3</td>
<td>42.1</td>
<td>8.7</td>
<td>8.7</td>
</tr>
<tr>
<td>15</td>
<td>47.5</td>
<td>21.5</td>
<td>7.5</td>
<td>57.6</td>
<td>9.7</td>
<td>9.3</td>
</tr>
<tr>
<td>20</td>
<td>68.0</td>
<td>37.5</td>
<td>8.3</td>
<td>84.7</td>
<td>14.7</td>
<td>10.0</td>
</tr>
<tr>
<td>25</td>
<td>92.7</td>
<td>48.8</td>
<td>14.2</td>
<td>117.2</td>
<td>21.6</td>
<td>13.6</td>
</tr>
<tr>
<td>30</td>
<td>114.8</td>
<td>66.4</td>
<td>23.2</td>
<td>163.0</td>
<td>28.3</td>
<td>19.0</td>
</tr>
</tbody>
</table>

* - Parasitic loop inductance

Notes:
- Measured $E_{OFF}$ includes the energy that charges the output capacitance ($E_{OSS}$), which will be dissipated during turn-on at next switching cycle for hard switching application.
- For resonant soft-switching topology, Energy stored in $C_{OSS}$ is recycled and should not be included in switching loss calculation. The actual $E_{OFF}$ can be calculated by:
  \[
  E_{OFF} = E_{OFF \, Measured} - \frac{1}{2} C_{O(ER)} \times V_{DS}^2
  \]
  Where $C_{O(ER)}$ is energy related capacitance @ $V_{DS}=400V$ and can be found on datasheet.
Preventing Miller turn-on

Miller turn-on – how to prevent it

1) Design for low pull-down impedance on the gate:
   • Select driver with low source $R_{OL}$
   • Optimize $R_{GON}$ in half bridge
   • Use small $R_{GOFF}$ for turn-off
   • Reduce gate loop inductance $L_G$

2) Adding external $C_{GS}$?
   • Provides additional miller current shunt path
   • Be careful when adding $C_{GS}$ to the gate:
     • Slow down switching; increases gate drive loss
     • *Potential gate oscillation combined with parasitic inductance → Ext. $C_{GS}$ provides low Z path for high-frequency gate current ringing*

2) Negative gate voltage?
   • Increase noise immunity against miller turn-on
   • Typical -2 to -3V is recommended
   • Reduce turn-off loss
   • Higher reverse conduction loss -> design trade-off
Using Clamping Diode

Clamping Diode

For gate driver with single output, a clamping diode is recommended

- High dV/dt at the Drain induces Miller Current flow (Source-to-Gate)
- $R_{G,OFF}$ does not help with high dV/dt (i.e., blocked by series Diode)
- Negative voltage spike increases with higher $R_{G,ON}$
- Use a fast schottky diode or zener between G and S:
  - Be careful with gate ringing induced by zener diode

Miller Current flow, $-dV/dt$ (No Diode)

With Clamping Diode

Clamping Diode

- $R_{ON}=20\Omega$, no $D_{CLAMP}$
  - $-13V$

- $R_{ON}=20\Omega$ with $D_{CLAMP}$
  - $-2V$
High side driver considerations

High side gate drive

- GaN enables fast switching \(dv/dt >100kV/us\):
  - Minimize Coupling capacitance \(C_{IO}\)
  - CM current via \(C_{IO}\) limits CMTI
- **Full Isolated gate drive:**
  - Best performance
  - Isolation power supply – Minimize inter-winding Capacitance
- **Bootstrap:**
  - Lower cost, simpler design
  - Post-regulation or voltage clamping is required after bootstrap

**Note:**
*Watch for bootstrap HV diode power loss limit and recovery time for High-Frequency operation. Choose the HV diode with low \(C_J\) and fast recovery time. For switching frequency application > 500k-800kHz, isolated gate drive is recommended*
Bootstrap Design

Bootstrap circuit design

Bootstrap with post-regulation

Using Zener for clamping

Bootstrap Design Example

Bootstrap voltage not tightly regulated: biased by $V_{SD} + V_{SW}$ noise
Preventing Oscillations

Gate drive stability – parasitic oscillation

What causes the gate oscillation?
• Common Source Inductance (CSI) \( L_{CS} \) Feedback path from power loop to gate loop \( (\text{di/dt}) \)
• Capacitive coupling via miller capacitor \( C_{GD} \) \( (\text{dv/dt}) \)
• Uncontrolled oscillation if feedback phase shift is -180deg
• \( L_{CS} \) and power loop Inductance should be minimized

How to prevent parasitic oscillation
• Reduce \( L_{CS} \), \( L_G \) and minimize external \( C_{GD} \)
• Slow down turn-on to reduce \( \text{dv/dt} \) and gate ringing
• Reduce additional \( C_{GS} \) -> high frequency path for gate current ringing
• Add small ferrite bead in series with \( R_G \) if oscillation observed:
  • Damp high frequency current ringing
  • Use a small SMD ferrite bead \( (Z=10-20) \)
Parasitic oscillation in half bridge

- Use double pulse tester as example: Q1 is synchronous and Q2 is active control device
- Q2 gate affects the Q1 gate stability with the presence of parasitic inductances
- Q2 switching noise couples to Q1 gate loop by parasitic inductance $Ls_1$ ($L \cdot \frac{di}{dt}$)
- Q1 Gate is OFF when Q2 is switched: Potential uncontrolled oscillation on half bridge if Q1 gate high frequency current ringing is not damped properly (Too low Z in turn-off drive path)
- Adding drive pull-down impedance $Z_{GATE}$ (Increasing $R_{GOFF}$ and/or inserting a small ferrite bead) damps the gate current ringing and improves the half bridge switching stability
Parasitic oscillation in half bridge

GS66504B 400V/10A Turn-off gate oscillation
Q1: $R_{\text{GOFF}}=3.3\Omega$; Q2: $R_G=15\Omega$ / $3.3\Omega$

No oscillation observed at 400V/10A switching
Q1 $R_{\text{GOFF}}=3.3\Omega$ + Ferrite bead; Q2: $R_G=15\Omega$ / $3.3\Omega$
Driver Selection

- Basics
- Design considerations
  - Driver selection
- Design examples
- PCB Layout
- Switching Testing results
Gate Driver selection

Select right gate driver for GaN E-HEMT

Non-isolated single gate driver:

**Minimum requirement:**
- Must operate at 5-6.5V gate drive
- Low pull-down output impedance: $R_{OL} \leq 2\Omega$
- 2A or higher peak drive current for robust turn-off
- Low inductance SMT package

**Preferred:**
- Separate pull-up/down drive output pins
- $\leq 1\Omega$ pull-down impedance
- Propagation delay $< 20\text{ns}$
- Integrated LDO for regulated 5-6V gate drive
- High frequency capability (>1MHz)

Isolator / Isolated gate driver

**CMTI rating:**
- GaN switches fast: 50-100kV/us $dv/dt$ at switching node is common
- High CMTI is required for 650V: 50kV/us is typical, 100-200kV/us preferred.

**High $F_{sw}$ and minimum dead time:**
- Good delay matching between high and low sides:
  - 650V application w/ isolated driver: 50-100ns, $\leq 50\text{ns}$ preferred
  - 100V application w/o isolated: $< 20\text{ns}$ preferred.
GaN Systems 650V E-HEMTs can be driven by many standard gate drivers

**Non-isolated low side single gate drivers:**
- **Recommend LM5114/UCC27511/MAX5048C:**
  - Separate source/sink outputs
  - Footprint compatible
  - Low $T_{\text{prod}}$ and low pull-down resistance
- Other lab tested compatible gate drivers:
  - FAN3122
  - FAN3224/FAN3225 (dual)
  - MCP1407/TC4422/IXDN609SI/LTC4441

**Integrated isolated gate drivers**
- half bridge gate drivers (footprint compatible):
  - SiLab **Si8273/4** (Use 4V UVLO for 6V drive, **Recommended for high CMTI rating 200kV/us**)
  - SiLab **Si8233AD** (UVLO= 6V for 6.5V gate drive)
  - Analog device **ADuM4223A** (UVLO = 4.1V)
- Isolated single gate driver:
  - **Recommended:** SiLab **Si8271** (4V UVLO for 6V drive, 200kV/us CMTI rating)
  - SiLab **Si8261BAC** (6.3V UVLO for 6.5V gate drive)

**Isolators (use with low side gate drivers):**
- SiLab **Si8610**: Recommended for High CMTI (lab tested 150V/ns) and low $T_{\text{prod}}$, requires 5V VCC
- New SiLab **Si862xxT** features >100kV/us CMTI rating
- Avago High CMR opto-coupler **ACPL-W483**: No 5V needed / Longer propagation delay and lower CMTI rating / 5kVrms reinforced insulation: for industrial application inverter, 3ph motor drive
SiLabs Si827x Series for 650V GaN E-HEMT

New Silicon Labs Si827x series isolated gate driver offers high CMTI dv/dt rating and low UVLO for GaN E-HEMTs:

- 4V UVLO for 5-6V optimum gate drive
- Separate Source/sink drive outputs (Si8271)
- 4A peak current
- High dv/dt immunity: $200\text{kV/\mu s}$ CMTI, $400\text{kV/\mu s}$ latch-up

Recommended P/N for GaN E-HEMT (4V UVLO):

- **Si8271BG-IS**: Single, split drive outputs
- **Si8273GB-IS1/IM**: High Side / Low Side
- **Si8274GB1-IS1/IM**: PWM with DT Adj.
- **Si8275GB-IS1/IM**: Dual
Recommended gate drivers - 100V GaN E-HEMT

**Gate driver for 100V Application:**

**Single/dual gate driver:**
- Recommend: **LM5114/FAN3122/FAN3225**
- Any standard MOSFET driver that supports 5-6V gate drive
- Secondary Synchronous Rectification

**Half bridge gate driver:**
- **For 48V Sync Buck, motor drive / inverter**
- No isolation required
- Dead time loss is critical: Minimize dead time
- TI **LM5113** (5V VCC, recommended for good propagation delay matching)
- Linear Tech **LTC4444-5** (Synchronous MOSFET driver, 5-6V VCC)

**Compatible Controllers:**
- **LTC3890/LTC3891** (60V Synchronous step-down controller, dual/single phase)
- **TPS40490** (5-60V Synchronous PWM Buck Controller)
Design Examples

- Basics
- Design considerations
- Driver selection
- Design examples
- PCB Layout
- Switching Testing results
650V Gate Drive Design Example 1

650V Half bridge fully isolated gate driver design reference (LM5114 + Si8610)

NOTE - UNLESS OTHERWISE SPECIFIED
1 - ALL SMD CAPACITORS AND RESISTORS ARE 0603 SIZE
2 - SMD CAPACITORS ARE 25V RATED 10%
650V Half bridge gate driver design using Si8273GB (footprint compatible with ADuM4223)

NOTES - UNLESS OTHERWISE SPECIFIED
1 - SMD CAPACITORS AND RESISTORS ARE 0603 SIZE
650V Gate Drive Design Example 3

650V Half bridge gate driver design (Si8271GB-IS w/ Isolated DC/DC)
FB1: 15ohm@100MHz
D1: PMEG2010
D2: 6.8V 200mW Zener diode SOD323 (MMSZ5235BS-7-F)

Full schematics and Gerber files can be found at: http://www.gansystems.com/gs66508t-evbhb.php
LM5113-based half bridge power stage (GS61008P), VDRV=+5V
For half bridge-based application: Sync. Buck, motor drive/inverter

Recommended Gate resistor:
- $R1/R3 = 4.7 \, \Omega$
- $R2/R4 = 2\, \Omega$

Minimize this loop
PCB Layout

- Basics
- Design considerations
- Driver selection
- Design examples

- PCB Layout

- Switching Testing results
**C\textsubscript{DG}:** drain-to-gate coupling capacitance
- Capacitive noise coupling
- Avoid overlapping between drain and gate drive copper pour/track

**L\textsubscript{CS}:** Common source Inductance:
- Gate ringing / oscillation
- Slow down switching
- Critical for gate drive stability
- Use kelvin connection to source

**L\textsubscript{DRAIN}/L\textsubscript{SOURCE}:** Power Loop Inductance:
- Drain voltage overshoot
- Turn-on/of drain voltage/current ringing
- Minimize power loop length and place decoupling Cap close to power device

**L\textsubscript{GATE}:** Gate loop inductance
- Gate signal over/undershoot
- Miller turn-on
- Place driver close to GaN FET to minimize gate loop

![Diagram of GaN FET with parasitic elements labeled](image.jpg)
1. **Reduce common source inductance**
   - Reference gate return ground to the source pad using Kelvin connection. For GS6xxx8P and GS66508B package use “SS” pin.
   - Increase $R_G$ or use ferrite bead on gate if gate oscillation is observed

2. **Optimize gate drive loop:**
   - Place driver close to GaN FET
   - Minimize the gate drive loop area and length

3. **Optimize power loop inductance:**
   - Use tight layout to minimize power loop length
   - Place decoupling capacitors as close as possible.

4. **Design for high dv/dt**
   - Minimize noise coupling due to PCB parasitic capacitance
   - Minimize overlapping between drain side power connection and gate drive signal track.

5. **Optimize thermal performance (B&P type package):**
   - Design for low thermal resistance using thermal vias and Cu. Pours
No Wire Bonds: ultra-low Inductance and much higher Manufacturing Reliability

Thick RDL & top Copper: extremely low $R_{ON}$

Embedded Package using high-$T_G$ material

Overall design achieves optimized Thermals
Bottom side $\text{GaNpx}^\text{TM}$ “P” & “B” Packages

- B package: create kelvin source on PCB
- P package: use SS pin
- Thermal pad connect to Source
- Use thermal vias for PCB cooling

For P package:
Always connect thermal pad to Source for optimum performance.

\[ \begin{align*}
\text{GS66508P} & \quad \text{GS66502/04B} \\
\text{Gate} & \quad \text{Gate} \\
\text{Driver} & \quad \text{Driver} \\
\text{Source} & \quad \text{Thermal Pad} \\
\text{G} & \quad \text{S} \\
\text{SS} & \quad \text{TPAD} \\
\text{Drain} & \quad \text{Drain} \\
\end{align*} \]
Half bridge Layout Examples 1

GS66508P Half bridge – (Si8261)

Component Side

Bottom Side

Solder Mask pulled-back:
- Improves thermal performance
- Allows Heat Sink attachment

Spacing for HV isolation
GS66508P Evaluation Board Layout Example

Half bridge Layout Examples 2

GS66508P Half bridge daughter board (isolated gate drive)

Top (component) layer

Internal Layer 1
GS66508P Half Bridge Daughter Board Layout Example

Half bridge Layout Examples 2

GS66508P Half bridge daughter board

Internal layer 2

Bottom layer
GaNpx™ “T” designed for higher-power Applications with Top-Side Heat-Sinking and lower $\Theta_{JA}$
Top side cooled GaNpx™ “T” series packages

- Low inductance package design with excellent thermal performance
- Dual gate (symmetric, internally connected) for easier layout
- Use the gate on driver side and keep the other floating, or
- Connect both gates for lower $L_{\text{gate}}$ if layout allows

Dual Gate Pins

Thermal pad (internally connected to Source)

Decoupling Capacitors

GaN E-HEMTs

TIM

Heat Sink

Vias for low loop inductance

Floating high side gate drive

Decoupling Capacitors

Via’s to gate drive outputs on the opposite side
100V GS61008P Half bridge Layout
TI LM5133 half bridge gate driver
Switching Test Results

- Basics
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Double pulse Switching Test

- **Gate Drive design:**
  - GS66508T in half bridge
  - Si8610 plus LM5114
  - Isolated Gate Drive supply
  - $R_{ON} = 10\Omega / R_{OFF} = 2\Omega$

- **Tested at 400V, 35A Hard-Switching**

![Diagram of gate drive design](image)
Low inductance GaNPx T package achieves minimum $V_{DS}$ overshoot and $V_{GS}$ ringing (No kelvin source)
Gate drive waveforms

Gate Drive Switching Waveforms

- Inductive load pulse testing to verify gate driver stability over the current range
- Si8261BAC Gate driver (EVAL BOARD)
- $R_{\text{ON}}=25\Omega$ / $R_{\text{OFF}}=0\Omega$
- Use Ferrite bead 15R@100MHz
- No oscillation and minimum drain voltage overshoot
Clean turn-on and off switching waveforms with well controlled gate ringing and miller voltage

Clean waveforms – controlled Miller voltage

Hard Switching HS Turn-on (400V/25A)

- $V_{\text{miller}} \approx 1.0V$
- $V_{\text{GSL}}$
- $V_{DS}$
- $V_{DS \text{ tr}} = 8.6\text{ns} (\sim 47V/ns)$

Hard Switching HS Turn-off (400V/31A)

- $V_{DS \text{ tr}} = 4.5\text{ns} (\sim 90V/ns)$
- $I_L$
- $V_{GSL}$
- $V_{DS}$
- $V_{GSD}$
Measuring Eon and Eoff

**GS66508P** $E_{\text{ON}}/E_{\text{OFF}}$ measurement waveforms (half bridge)
- Current shunt: T&M research SDN-414-10

400V/25A Turn-on switching loss energy $E_{\text{ON}} = 93\mu\text{J}$  
$R_{\text{GON}} = 10\Omega$

400V/25A Turn-off switching loss energy $E_{\text{OFF}} = 49\mu\text{J}$  
$R_{\text{GOFF}} = 10\Omega$