

# Using “Normally on” JFETs in Power Systems

*A “normally on” device can get short shrift at times due to the negative turn off voltage requirement. Supply Voltage sequencing and single point failures tend to make designers skittish, and thus bypassing the die size/resistivity advantages of “normally on” devices, and the capacitive advantages that go along with using devices with smaller die size.*

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The approach to this dilemma is to not only create a “normally off” device by adding additional circuitry, but to do so in order to create advantages over a traditional “off” device. Parity is not enough. A designer needs an incentive. In the context of wide bandgap SiC, this article will highlight several circuit configurations that deliver performance improvements over their corresponding SiC enhancement devices that can give the circuit designer an advantage.

## “Normally on” to “Normally off”

The classic way to convert a “normally on” device to “normally off” is the well understood cascode configuration, as shown in Figure 1. A low Voltage device (typically 25 to 30 Volts) is placed in series with a “normally on” high Voltage device (in this example a JFET), and by connecting the Gate – Source and Drain-Source of the two devices, as shown, the JFET VGS is now the inverse of the MOSFET VDS. The JFET will now turn off whenever the MOSFET VDS increases to the [JFET Vth]. The addition of a Low Voltage MOSFET has created a high Voltage normally “off” device.

A MOSFET structure also forms an intrinsic diode, which is critical to switching inductive loads in Bridge configurations. A discrete JFET does not have a drain-source intrinsic diode, so how does the cascode solve this issue? The cascode is a series combination of enhancement (Si MOSFET) and depletion device (SiC JFET). When the cascode MOSFET’s intrinsic diode conducts, the JFET is fully “on”, and can conduct a current from source to drain, as the JFET VGS is [MOSFET VSD]. The addition of a low Voltage MOSFET creates an electrical path for switching inductive loads.

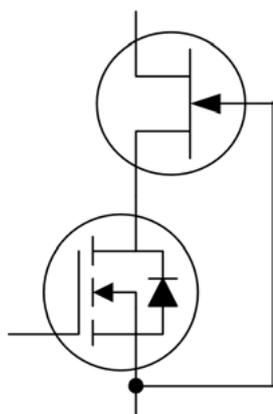


Figure 1: Cascode Circuit

## Comparing Cascode and MOSFET in the context of Wide Bandgap

It has been shown that a cascode configuration can reach functional parity with an enhancement mode device, but what of the “ease of use” and “performance”?

### Gate Drive

In SiC, Gate drive is a differentiator between cascode and enhancement mode devices. In a cascode configuration, the control device is a low Voltage MOSFET, so the same Voltage levels (0 to 10V) can be used for driving the cascode. Since the JFET is the largest percentage of resistance, the threshold of the

MOSFET can be set high to give some relief with respect to threshold decrease with temperature or high dV/dt conditions. The cascode MOSFET’s miller capacitor will only see low Voltage excursions (< 30V).

SiC MOSFETs may have low thresholds (2.8V typ.), but to reach advertised RDS, the VGS Voltages must typically reach 18 to 20 Volts. This is outside the range of standard MOSFETs where RDS is rated at 10V VGS, and typical drivers have an absolute maximum rating of 18V. The Gate Drive design of an 1.2kV SiC MOSFET must also take into account that the Miller capacitor will see the full dV/dt of the load Voltage, when put in context of the low VTH may require negative gate drive to insure the device is off during all conditions (-5V to +20V).

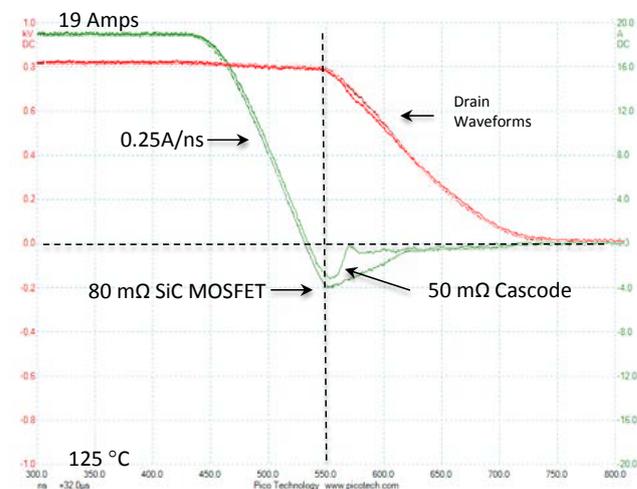


Figure 2: QRR Comparison (SiC MOSFET,381Nc vs. Cascode 155 nC)

## QRR, Reverse Recovery

Switching inductive loads in Bridge configurations requires an intrinsic diode to transition from passing current to blocking Voltage every cycle. This reverse recovery (QRR) generates losses that impact system efficiency. To compare cascode against a single device, the reverse recovery of an 80 mΩ SiC MOSFET is compared against the cascode of a 45 mΩ JFET and 5 mΩ MOSFET at 125 °C (Figure 2). The reverse recovery of the SiC MOSFET is 2.5x that of the cascode, and that is a 50 mOhm cascode solution vs. 80 mOhm MOSFET. Putting QRR in context, a SiC MOSFET’s QRR will essentially triple over a 100 °C rise, where a cascode’s QRR will increase by only 10%.

**Cascode overview**

In short, a designer using cascode will be able to utilize standard Si MOSFET drivers, and have lower reverse recovery losses than using a SiC MOSFET.

**Stacking “Normally” On Devices**

The above paragraphs went over the advantages one can achieve by implementing a cascode configuration with a “normally on” JFET. This same approach can also be used to create higher Voltage devices. In Figure 3, a super cascode configuration is created by putting a series of low cost silicon avalanche diodes in parallel with a series of “normally on” JFETs.

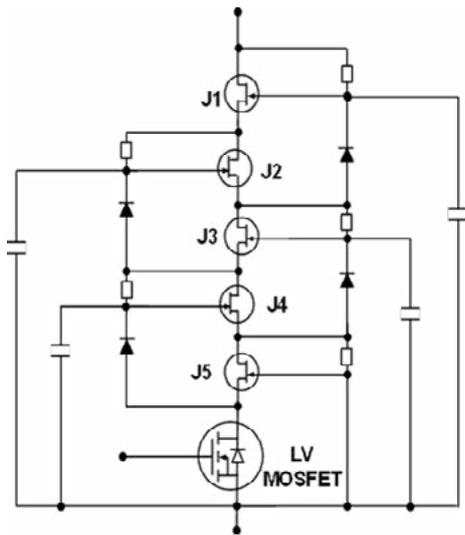


Figure 3: Super Cascode

The operation of the super cascode is similar to the standard cascode, but with the switching happening sequentially. The Low Voltage MOSFET turns “on”, which turns “on” its corresponding JFET and this process, moves up the chain until all devices are fully “on”.

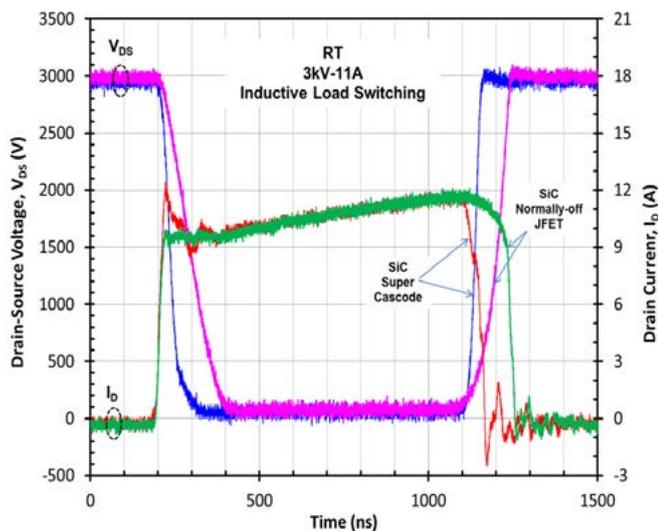
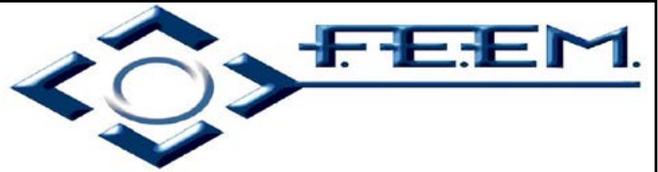


Figure 4: Super Cascode vs. Single device

For turn “off”, the silicon diodes’ breakdown Voltages fix the maximum Drain-Source Voltage of each JFET. The MOSFET turns “off” and its drain Voltage increases until it reverse bias’s the gate of the above JFET. Devices continue to turn “off” up the chain until all the devices are off.



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By using a “normally on” device, Voltage is naturally shared and there is no need for complicated gate drive schemes required by “normally off” devices.

The sequencing may sound slow, so how does this compare against a single high Voltage device? In Figure 4, a single 6.5 kV, 300mΩ “normally off” JFET is compared against five stacked 1.2kV, 45 mOhm “normally on” JFETs in a super cascode configuration (~ 230 MOhms) switching 11 Amps.

It is apparent that the switching times of the super cascode are actually faster than the single device. The turn on and turn off energy losses are measured and the super cascode turn “on” loss is less than half of the single device (1.2 mJ vs. 2.7 mJ), and the turn “off” loss of the super cascode is approximately one third of the single device (0.53 mJ vs. 1.54 mJ), even though it has 25% lower on resistance.

The super cascode switches faster and has lower dynamic losses, but it also has an economic advantage. The cost of epi increases with breakdown Voltage to the point that 80% of a 6.5kV device die cost can be in epi. The use of 1.2kV devices gives designers flexibility in tailoring their mid Voltage requirements (breakdown and RDS), but also allows them to take advantage of the higher volume/price curve of 1.2kV.

**Summary**

There are significantly advantages in gate drive simplicity and reverse recovery performance when using “normally on” JFETs in cascode. Super cascode provides faster switching performance and a lower cost path than traditional single die approaches. It is hoped that designers will give “normally on” devices their due by exploring the trade-offs and advantages in meeting their system requirements.

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