Switching Behavior of USCi's SiC Cascodes

The co-packaged cascode device, combining a Silicon low voltage FET with a trench vertical SiC normally-on JFET, was recently introduced by United Silicon Carbide. This device has several benefits, including the ability to use standard 10V or 12V gate drive, high Vth (4.5V), fast temperature independent switching, avalanche and short circuit-ratings and an excellent built-in diode with a low forward drop and recovery charge.

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This article examines the hard switching turn-on and turn-off mechanisms in this device, to give the users some insight into how these devices differ from MOSFETs and IGBTs.

Trench JFET Structure

Figure 1 shows the schematic cell structure of the trench JFET. The low on-resistance derives from the vertical channel that repeats with a high cell density, creating a short path between the source and drain contacts via the channel and drift regions. The drift region doping and thickness are determined by the desired voltage rating. The trench JFET does not contain a built-in body diode, or any parasitic NPN transistor. Its controlling channel is formed by pn-junction and is purely vertical, having no critical gate-oxide or any surface conduction path. As illustrated in Figure 1, a pn-junction diode is formed between the gate-source and the gate-drain regions. By controlling the opening width of the vertical channel, a normally-on JFET can be implemented. The normally-on JFET typically has a threshold voltage (V_{THJ}) of -6V. To achieve the rated blocking capability, usually a reverse bias of -15V to -20V is applied between the gate and source contacts [1], which is sufficient to deplete the channel region and form a potential barrier between the drain and source. If a drain voltage is now applied, the JFET will block this voltage by depleting the drift region.

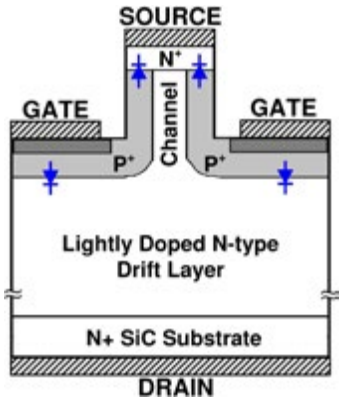

Figure 1: Cell structure of SiC trench JFET

In the on-state, if the gate-source voltage is 0V, the channel region is not depleted. A low resistance current path exists directly from the source to the drain. As the current increases, the potential at the drain side of the channel increases. When the potential difference between the drain and the gate reaches the 6V threshold, the channel pinches off and the current saturates.

Co-packaged SiC Cascode Structure

Figure 2a shows the structure of the co-packaged SiC cascode, where a customized low-voltage silicon MOSFET is connected in series with a SiC normally-on JFET to implement a normally-off device [2, 3]. The equivalent circuit of the cascode is shown in Figure 2b. Figure 3 shows the typical on-state characteristics of 1200V-60mΩ SiC co-packaged cascode. The cascode device has a threshold voltage (V_{TH}) of 4.5V and is fully enhanced for the gate voltage (V_{GS}) values above 10V.

The cascode is switched on by turning on the low-voltage MOSFET. Since the MOSFET drain-source voltage drop (V_{DS}) is small (I_D*$R_{DS(ON)}$), the JFET gate-source voltage (V_{GS}) is near 0V in the

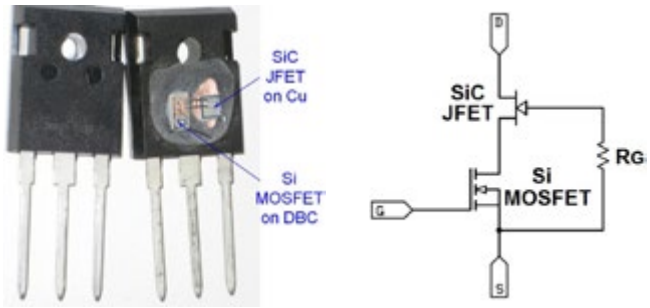

Figure 2: Co-packaged SiC cascode in TO-247 package (a) and equivalent circuit (b)

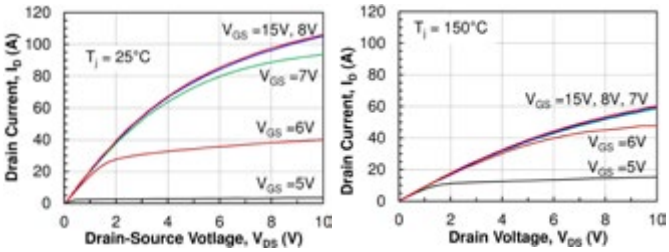

Figure 3: Typical on-state characteristics of 1200V-60mΩ co-packaged SiC cascode at a junction temperature of 25°C (a) and 150°C (b).

on-state and the channel can conduct. When the low voltage MOSFET is turned off, the drain potential rises. The MOSFET V_{DS} appears as a negative V_{GS} on the SiC JFET, turning it off.

Inductive Switching Behavior

For the cascode devices, the turn-on tends to be significantly slower than the turn-off, so the commonly recommended gate drive circuit uses a low gate resistor for turn-on (R_{G_ON}: 0-4.7Ω), and a large gate resistor for turn-off (R_{G_OFF}: 10-50Ω) as shown in Figure 4. A ferrite bead can be used at the gate lead to reduce ringing. PCB layout techniques that help to minimize the gate-drain coupling due to stray capacitances are necessary because of the high dv/dt and di/dt that can occur in the SiC cascode during turn-off.

To aid with the discussion that follows, a term V_{GPJ} referred as the plateau voltage is defined for the JFET:

$$V_{GPJ}=V_{THJ}+I_D/g_{mJ} \quad (1)$$

This term corresponds to the voltage seen in the gate-charge curve at a load current of I_D. Here, g_{mJ} is the JFET trans-conductance and V_{THJ} is the JFET threshold voltage.

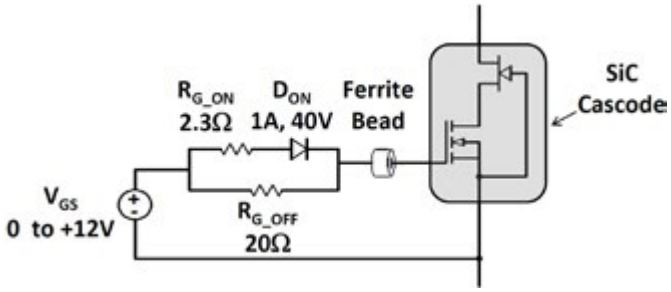

Figure 4: Recommended gate drive for SiC cascode

Turn-on: Figure 5a shows the typical turn-on waveforms of the SiC cascode. The turn-on process is initiated by raising the gate-source voltage (V_{GS_M}) of the MOSFET, then the drain-source voltage (V_{DS_M}) of the MOSFET falls and the gate-source voltage (V_{GS_J}) of the JFET increases because the V_{DS_M} is equal to $-V_{GS\_J}$. The V_{DS_M} holds at a value close to $-V_{GPJ}$, meaning that the V_{GS_J} of the JFET is held at the plateau voltage V_{GPJ} which is just sufficient for the JFET to handle the load current. The current ramps up in the JFET and the MOSFET simultaneously. The MOSFET V_{GS_M} is still at its plateau voltage at this stage. Once the current reaches the load current (plus any extra current to recover the freewheeling diode), the MOSFET V_{DS_M} falls towards $I_D*R_{DS(ON)}$, and finally, the cascode V_{DS} falls.

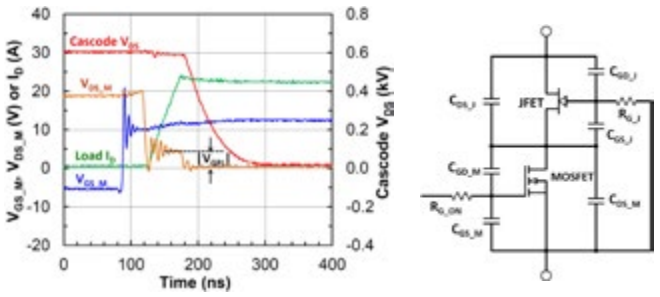

Figure 5: Measured turn-on waveforms of a 1200V SiC cascode under an inductive load condition (a) and equivalent circuit of the cascode (b)

The turn-on di/dt is limited by stray inductance at the MOSFET source and between the MOSFET drain and JFET source. It can be controlled well by the resistor (R_{G_ON}) in series with the MOSFET gate. The turn-on dv/dt can be better understood using the equivalent circuit as depicted in Figure 5b, where the stray inductances are not included for clarity. If the R_{G_ON} is small, the MOSFET turns on fast. The discharge rate of the drain-source voltage of the cascode is mainly determined by the discharge rate of the gate-drain capacitance (C_{GD_J}) of the JFET because the JFET has near zero drain-source capacitance ($C_{DS\_J} << C_{GD\_J}$). The load current is flowing through the conducting channel of the JFET while the voltage falls. Displacement current through the internal gate resistor (R_{G_J}) of the JFET discharges the C_{GD_J} and drives the JFET gate to a more negative potential. Since the JFET gate cannot be driven too far negative without choking off the channel load current, the JFET V_{GS_J} will stay at V_{GPJ}. Therefore the maximum current through R_{G_J} will set the maximum value of the turn-on dv/dt based on the following equation:

$$(V_{GPJ}- I_D*R_{DS(ON)})/R_{G\_J} = C_{GD\_J}*dv/dt \quad (2)$$

In this manner, the gate resistance R_{G_J} of the JFET can be used to slow down the turn-on dv/dt. On the other hand, a lower R_{G_J} and higher $|V_{GPJ}|$ value (more negative V_{THJ} for the JFET) can be used to obtain a faster turn-on.

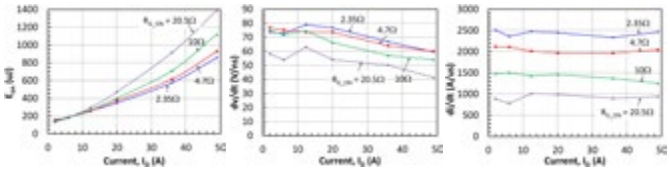

Figure 6: Measured turn-on energy loss (a), dv/dt rate (b) and di/dt rate of the 1200V-60mΩ SiC cascodes (UJC1206K) under a 600V-bus inductive load condition with the same device as a freewheeling diode.

Figure 6 shows the effects of the turn-on gate resistor R_{G_ON} on the energy loss, dv/dt rate and di/dt rate of USCi's SiC cascode (UJC1206K) during the turn-on transient. For low values of R_{G_ON}, the dv/dt is controlled by equation (2). For large values of R_{G_ON}, dv/dt can be controlled by slowing the transition of the MOSFET drain-source voltage (V_{DS_M}), which is equivalent to slowing down the gate turn-on voltage of the JFET.

Turn-off: Figure 7 shows the typical turn-off waveforms of the SiC cascode. The turn-off transient is initiated by turning off the MOSFET gate. After a delay (determined by $R_{G\_OFF}*C_{ISS\_MOSFET}$), the drain-source voltage (V_{DS_M}) of the MOSFET rises. The V_{DS_M} is clamped to the avalanche breakdown voltage of the MOSFET and is seen to hold there during the period the drain-source voltage of the cascode rises. This generates a negative voltage between the gate and source of the JFET to turn off the JFET. Since the JFET still conducts the load current during the voltage rise, the gate-source voltage V_{GS_J} of the JFET has to stay at the plateau voltage VGPJ in order to sustain that current. The drain-source capacitance C_{DS_J} of the JFET is nearly zero, so there is very little current flowing through that path to the MOSFET gate, meaning that the cascode has very little Miller current. As the drain-source voltage of the cascode rises, its slope (dv/dt) is again dominated by the charging rate of C_{GD_J} through the JFET internal gate resistor R_{G_J}. The maximum current that can pass through R_{G_J} is given by:

$$I_G(R_{G\_J}) = \{BV_{(MOSFET)}-V_{GPJ}\} / R_{G\_J} = C_{GD\_J}*dv/dt \quad (3)$$

Again, the maximum dv/dt can be limited by controlling R_{G_J}. The turn-off dv/dt can also be reduced by using the MOSFET with a lower avalanche breakdown voltage and the JFET with a larger plateau voltage V_{GPJ} (more negative threshold).

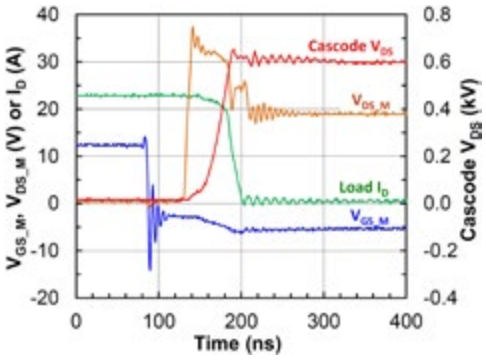

Figure 7: Measured turn-off waveforms of a 1200V SiC cascode under an inductive load condition

Once the drain-source voltage of the cascode reaches the bus voltage, the current rapidly decays as the JFET gate discharges. The discharge time constant depends on R_{G_J}*C_{GS_J}, and is also slowed down by the common source parasitic inductance in the gate loop of the JFET. The drain-source voltage of the MOSFET during the current fall in Figure 7 is set by its off-state value plus the voltage spike induced by the parasitic inductances between the drain and source terminals of the MOSFET. Once the current ramp is finished, the MOSFET V_{DS_M} stabilizes quickly at a voltage needed to hold the JFET off.

Figures 8 shows the effects of the turn-off gate resistor R_{G_OFF} on the energy loss, dv/dt rate and di/dt rate of USCi's SiC cascode (UJC1206K) during turn-off transient. For low values of R_{G_OFF}, the dv/dt is controlled by equation (3). For large values of R_{G_OFF}, dv/dt and di/dt can be controlled by slowing down the transition of the MOSFET drain-source voltage V_{DS_M}, which is equivalent to slowing down the turn-off gate voltage of the JFET. However, this comes at the cost of a longer delay time proportional to R_{G_OFF}*C_{iss_MOSFET}.

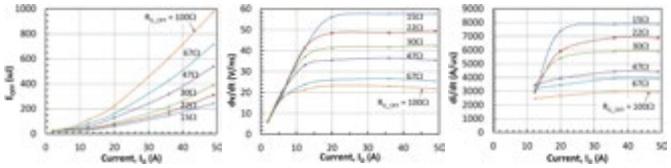

Figure 8: Measured turn-off energy loss (a), dv/dt rate (b) and di/dt rate of the 1200V-60mΩ SiC cascodes (UJC1206K) under a 600V-bus inductive load condition with the same device as a freewheeling diode

The low-voltage MOSFET used for USCi's SiC cascodes is custom designed to have a built-in voltage clamp in order to make it operate safely in avalanche mode. Figure 9 shows the general concept of how this is accomplished by creating a low breakdown region between cells to carry the entire breakdown current. USCI Cascodes are 100% avalanche tested at final test.

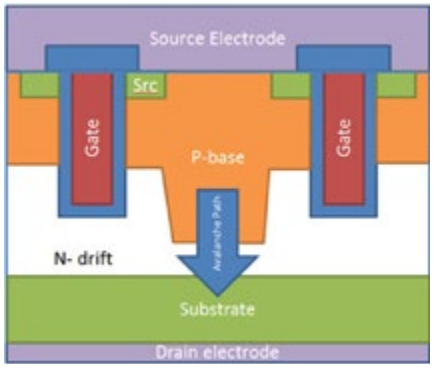

Figure 9: Low-voltage silicon MOSFET designed with an avalanche clamp to control cascode switching speed

During device development, stress tests are performed to ensure that all sampled devices pass 10^6 cycles of unclamped inductive switching (UIS). In addition, the MOSFET is qualified by the burn-in test when biased into avalanche for 1000hrs at a junction temperature of 150°C. As shown in Figure 10, negligible parameter shifts are observed after the burn-in test. The standalone MOSFETs are also tested to ensure that all sampled devices pass 10^6 cycles of UIS. With these precautions, the cascode can be used with the low-voltage MOSFET acting as the voltage clamp to limit its maximum turn-off speed.

ZVS Turn-on behavior: The ZVS turn-on behavior of the USCi cascode is also different from other cascode devices due to the fact that the trench JFET has almost zero drain-source capacitance C_{DS_J}. Consider the situation where the cascode voltage is rapidly decreasing to zero while the MOSFET is still off. Since C_{DS_J} is nearly zero, all the displacement current has to flow into the C_{GD_J} path. There is no voltage balancing concern between C_{DS_J} and the capacitances tied to the drain of the MOSFET (C_{GD_M} + C_{DS_M} + C_{GS_J}) because the latter capacitance is much larger. This means that the accidental turn-on of the JFET due to high dv/dt [4, 5] can be avoided, making USCi's SiC cascodes very well suited for applications with ZVS turn-on and hard turn-off.

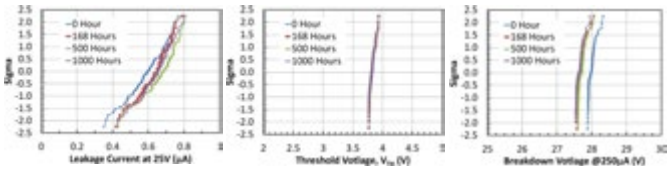

Figure 10: Measured shifts in the leakage current at 25V (a), threshold voltage (b), and breakdown voltage at 250μA (c) of the low-voltage silicon MOSFETs before and after 1000 hours of avalanche-mode burn-in at 150°C.

Summary

USCI's co-packaged cascode device offers ease of use benefits to power system designers, requiring minimal modification of existing designs from the gate drive standpoint, and reducing cost by eliminating the need for an anti-parallel SiC diode. The high speed turn-off behavior requires attention to layout to mitigate EMI issues, so as to extract maximum benefit from the fast switching speed of the cascode structure. Given the avalanche and short-circuit ruggedness of the device, along with its excellent body diode, the device is well suited to a wide range of high performance circuits. Parts may be purchased directly on USCi's website from May 1, 2015.

References

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