

Introduction

The performance improvements of Silicon Carbide switching devices compared against standard Silicon devices are well documented. What can be confusing are the drive requirements for the various SiC devices and the variation between suppliers. This document is designed to be used in conjunction with the data sheet to enable designers to confidently design with United Silicon Carbide (USCi) normally on xJ Series 1.2kV JFETs.

USCi Drive Voltages

USCi manufactures depletion mode JFET's that are commonly referred to as “normally on”. A typical USCi JFET has a threshold or “Gate cutoff Voltage” of -6 Volts. In Figure 1, The threshold Voltage is stable across temperature. This stability simplifies gate drive analysis with respect to a standard silicon device would have a 2 Volt swing over the equivalent temperature range.

The resistance of the device, $R_{DS(on)}$ is set by the Gate Source Voltage (V_{GS}). USCi rates the $R_{DS(on)}$ at $V_{GS} = +2$ Volts and $V_{GS} = 0$ Volts. The $V_{GS} = +2$ Volt rating is the lowest resistance specified for the device. One will not gain a performance advantage by driving the JFET above the +2V rating, but it will not harm the device either. The $V_{GS} = 0$ Volt rating is convenient for cascode, which will be covered in another note.

With respect to the positive voltage, there is a PN Junction that will forward bias above +2V, so it is advised to add a Gate resistor to limit the current in order to minimize any excess power dissipation. Figure 2 is a curve tracer plot of the JFET's Gate current without a limiting resistor. When driving the JFET above +2V, it is recommended to use a 3.3V or 5 V level with a Gate resistor.

As the threshold is centered at -6 Volts with a six sigma range of -4V to -10 Volts, it is a general recommendation to use -15V to insure a good stable turn off. This should account for layout inductances and less chance of accidental turn on or turn off due to high dv/dt's.

In Figure 3 a gate resistor is added to allow a +5V rail to be used in driving a JFET in a high frequency boost converter.

Overall Device Robustness

The die of a USCi JFET can be operated to 250 °C. In die form the device can be avalanche or short circuited to any energy level as long as the die temperature is kept below 250 °C, the current ratings of assembly are met and no other abs. max. values are violated.

With respect to molded packages (TO-247), for long term reliability the above applies, but the junction temperature should be kept below 175 °C.

From a die perspective, it is possible to operate above 250 °C, and once again, any systems requiring operation above these conditions, please contact USCi.

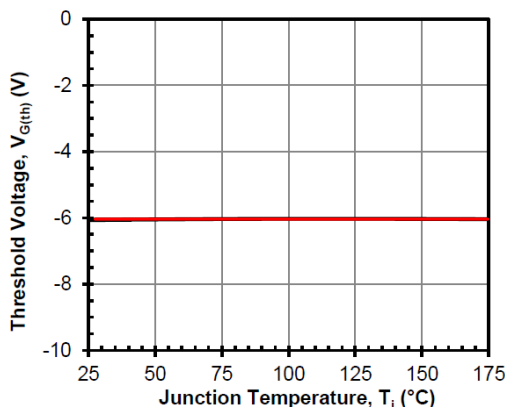


Figure 1: JFET Threshold Voltage vs. T_j

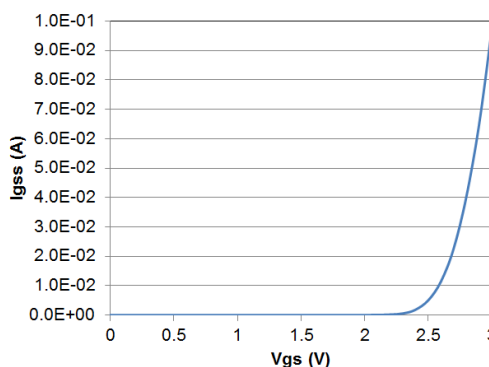


Figure 2: Gate Current vs. V_{GS} Voltage

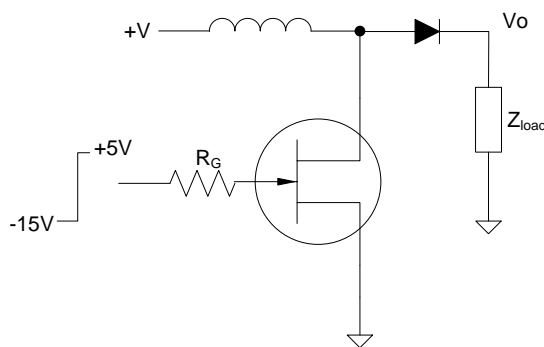


Figure 3: JFET in a Boost Converter

RDS(on) with respect to Temperature

The $R_{DS(on)}$ of a USCi JFETs changes similarly to a high Voltage Silicon MOSFET with respect to temperature and current. From 25 °C to 175 °C the $R_{DS(on)}$ will increase approximately 3x in value. Figure 4 combines the current and temperature information for USCi’s 1.2 kV, 45 mOhm JFET (UJN1205K).

It is important to take in these temperature effects when calculating the system’s conduction losses

Switching Inductive Loads

The vast majority of applications using silicon carbide devices switch inductive loads. Since inductive switching can involve clamping inductive energy there are a few items to point out. The first is that the JFETs are bi-directional, so they can be utilized in synchronous rectification. The dead-time in synchronous rectification, however requires the addition of a diode.

Since the JFET does not have an intrinsic diode, one must be added to the circuit. Another option would be to operate the JFET in the cascode configuration. The cascode configuration is dealt with in another application note, so the diode inductive clamp example will be shown here.

20 Amps is switched through a 500µH inductor across 800 Volts using the classic inductor switching circuit shown in Figure 5. A USCi’s 45 mOhm 1.2 kV JFET (UJN1205K) is the switching device and 1.2 kV JBS diode (UJ2D1210T) is used to clamp the energy stored in the inductor during the off time. The 25 °C and 250 °C data are shown in Figure 6 and 7 respectively.

The turn on di/dt is 1.5 A/nsec., and the turn off di/dt is 0.4 A/nsec. This is stable across a 200 °C rise in junction temperature. The device is being driven from +2V to -15V Volts with a 4.7 Ohm gate resistor.

Gate Charge

The previous waveforms are all generated with a simple gate drive. A resistor is used to limit the peak gate current, so as not to saturate the driver, and drive Voltages are set to insure good enhancement and no accidental turn on. Due to EMI, layout and/or load impedances, many designs require asymmetrical switching. This overview cannot go through all the options, but one of the best data sheet specifications for sizing turn on and turn off with respect to switching characteristics times are the gate charge values.

The Q_{GS} value determines the turn on delay. For the UJN1205K this is only 10nC, so the device is going to have minimum turn on time.

Q_{GD} is when the actual switching will take place, and with the UJN1205K this is 74 nC and is the plateau in the gate charge curve. Sizing the drive current for the plateau will give control over the rise and fall times. When attempting to speed up or slow down switching times, accounting for Q_{GD} will deliver the best design. The remaining charge to reach Q_G , directly related to better enhancement and turn off delay. In the UJN1205K, the remaining 23nC is tied to the turn off delay. With symmetrical drive currents, turn off delay will be about twice the turn on delay.

Conclusion

This application note is an overview of United Silicon Carbide’s 1.2 kV normally on JFETs. They can be operated over a wide range of Gate Voltages, and the high temperature capability make them extremely rugged.

If there are any specific application questions that require an immediate response, please do not hesitate to contact USCi’s application group (jbendel@unitedsic.com).

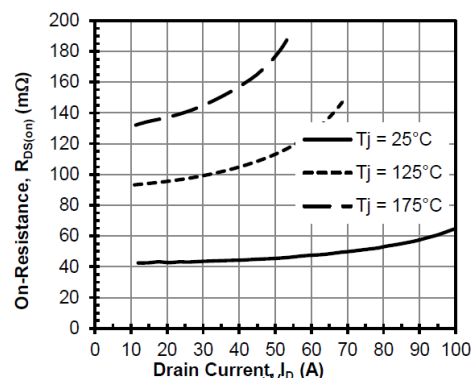


Figure 4: RDS(on) vs Drain Current vs. T_J

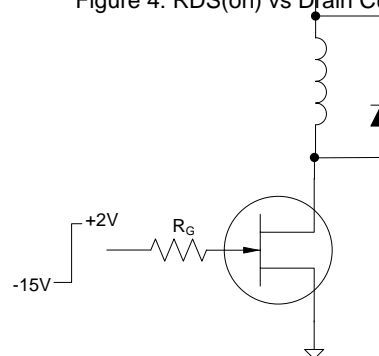


Figure 5: Inductive Switching Test

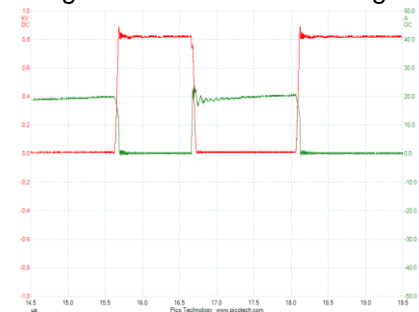


Figure 6: Inductive Switching Test 25°C

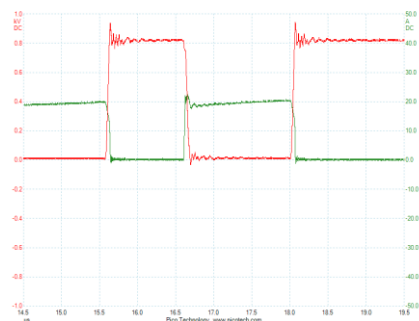


Figure 7: Inductive Switching Test 250°C